•		[A 15 46 -)
	Application No.	Applicant(s)
Nation of Allerent Hite.	10/814,955	JEON, JIN
Notice of Allowability	Examiner	Art Unit
	Thoi V. Duong	2871
The MAILING DATE of this communication appe All claims being allowable, PROSECUTION ON THE MERITS IS (herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIC	(OR REMAINS) CLOSED in or other appropriate commu GHTS. This application is s	this application. If not included inication will be mailed in due course. THIS
1. This communication is responsive to the amendment filed February 10, 2006.		
2. The allowed claim(s) is/are <u>1-35</u> .		
3. ☐ Acknowledgment is made of a claim for foreign priority un a) ☐ All b) ☐ Some* c) ☐ None of the:		or (f).
1. Certified copies of the priority documents have been received.		
2. Certified copies of the priority documents have been received in Application No. 10/051,701.		
3. Copies of the certified copies of the priority documents have been received in this national stage application from the		
International Bureau (PCT Rule 17.2(a)).		
* Certified copies not received:		
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		
4. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.		
5. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.		
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached		
1) hereto or 2) to Paper No./Mail Date		
(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date		
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).		
6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.		
Attachment(s) 1. Notice of References Cited (RTO 902)	5 □ Notice of In	formal Potent Application (PTO 152)
 Notice of References Cited (PTO-892) Notice of Draftperson's Patent Drawing Review (PTO-948) 		formal Patent Application (PTO-152) ummary (PTO-413),
2. Induce of Drauperson's Patent Drawing Review (P10-946)		
3. Information Disclosure Statements (PTO-1449 or PTO/SB/0	8), 7. Examiner's	Mail Date Amendment/Comment
Paper No./Mail Date 12/05/2005 4. Examiner's Comment Regarding Requirement for Deposit	8. Examiner's	Statement of Reasons for Allowance
of Biological Material	9. 🗌 Other	<u>-</u> -

Application/Control Number: 10/814,955

Art Unit: 2871

DETAILED ACTION

1. This office action is in response to the Amendment filed February 10, 2006.

Accordingly, claims 12, 31 and 33 were amended. Currently, claims 1-35 are pending in this application.

Allowable Subject Matter

2. Claims 1-35 are allowed.

The following is an examiner's statement of reasons for allowance: none of the prior art of record fairly suggests or shows all of the limitations as claimed. Specifically,

Re claims 1, 23 and 31, none of the prior art of record discloses, in combination with other limitations as claimed, a substrate (as well as a method for manufacturing the same) comprising:

a first insulating interlayer formed on the data pattern, the first insulating interlayer having a first contact hole for partially exposing the data electrode of the data pattern, a second contact hole for exposing a gate electrode of a first drive transistor of the peripheral region, and a third contact hole for exposing a data electrode of a second drive transistor of the peripheral region; and

an electrode pattern part formed on the first insulating interlayer, the electrode pattern part including a first electrode pattern in contact with a data electrode of the pixel region through the first contact hole, and a second electrode pattern connecting the partially exposed gate electrode of the first drive transistor with the exposed data electrode of the second drive transistor through the second and third contact holes.

Re claims 13 and 28, none of the prior art of record discloses, in combination with other limitations as claimed, a substrate (as well as a method for manufacturing the same) comprising:

a first insulating interlayer formed on the data pattem, the first insulating interlayer including a first contact hole for partially exposing the second electrode, a second contact hole for partially exposing the first electrode of the pixel region, a third contact hole for exposing a gate electrode of a first drive transistor of the peripheral region, and a fourth contact hole for exposing a data electrode of a second drive transistor of the peripheral region; and

an electrode pattern part formed on the first insulating interlayer, the electrode pattern part including a first electrode pattern coupled to a second electrode of the pixel region through the first contact hole, a second electrode pattern coupled to a first electrode of the pixel region through the second contact hole, and a third electrode pattern connecting the exposed gate electrode of the first drive transistor with the exposed data electrode of the second drive transistor through the third and fourth contact holes.

The most relevant reference, USPN 6,738,109 to Jin Jeon, discloses every limitations of the claimed invention. However, this reference is overcome by a terminal disclaimer has been filed on March 14, 2005 to overcome the nonstatutory double patenting rejection.

Art Unit: 2871

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (571) 272-2293.

Thoi Duong

04/23/2006

DUNG T. NGUYEN PRIMARY EXAMINER

Page 4